WAFER-LEVEL PACKAGING OF OPTOELECTRONIC DEVICES

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FIELD OF INVENTION

[0001] This invention relates to wafer-level packaging of optoelectronic devices.

DESCRIPTION OF RELATED ART

[0002] Optoelectronic (OE) devices are generally packaged as individual die. This means of assembly is often slow and labor intensive, resulting in higher product cost. Thus, what is needed is a method to improve the packaging of OE devices.

SUMMARY

[0003] In one embodiment of the invention, a wafer-level package includes a first wafer comprising a bonding pad, an optoelectronic device on the first wafer, and a second wafer comprising a gasket. The second wafer is attached to the first wafer by a bond between the gasket and the bonding pad.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figs. 1, 2, and 3 are cross-sections of a wafer-level package of an optoelectronic device in one embodiment of the invention.

[0005] Figs. 4, 5, and 6 are cross-sections of a wafer-level package of an optoelectronic device in another embodiment of the invention.

[0006] Use of the same reference symbols in different figures indicates similar or identical items. The cross-sectional figures are not drawn to scale and are only for illustrative purposes.

DETAILED DESCRIPTION

[0007] Figs. 1, 2, and 3 are cross-sections of a wafer-level package 100 (Fig. 3) for an optoelectronic device 102 in one embodiment of the invention. Referring to Fig. 1, package 100 includes a cap wafer 104 having gaskets 106 and 108, a via 110, and a cavity 112.

[0008] Cap wafer 104 can be silicon (Si), gallium arsenide (GaAs), indium phosphide (InP), or other similar materials.

[0009] Gasket 106 forms a perimeter around package 100 while gasket 108 forms a perimeter around via 110. Depending on the application, gasket 106 can include treads 114. In one embodiment, gaskets 106 and 108 are formed by masking and etching cap wafer 104. Alternatively, gaskets 106 and 108 can be deposited onto cap wafer 104 and then patterned by masking and etching or liftoff.

[0010] The surface of gaskets 106 and 108 are covered with a bonding layer 116. In one embodiment, bonding layer 116 is gold (Au) deposited by sputtering, evaporation, or plating, and patterned by masking and etching or liftoff. A barrier metal layer (not shown) can be formed between bonding layer 116 and gaskets 106 and 108 to act as a diffusion barrier and to improve adhesion between the bonding layer material and the cap wafer material.

[0011] Cavity 112 includes an angled surface 118. In one embodiment, cavity 112 is formed by masking and etching cap wafer 104. Surface 118 is covered with a reflective layer 120 to form a mirror 121. In one embodiment, reflective layer 120 is Au deposited by sputtering, evaporation, or plating, and patterned by masking and etching or liftoff. Like bonding layer 116, a barrier metal layer can be deposited between reflective layer 120 and surface 118 to act as a diffusion barrier and to improve adhesion. If bonding material 116 and reflective material 120 are the same material, they can be deposited at the same time.

[0012] Package 100 further includes a base wafer 118 having an integrated lens 113, a bonding pad 120, and a contact pad 122. Base wafer 118 can be Si, GaAs, InP, or other similar materials.

[0013] In one embodiment, integrated lens 113 is a diffractive optical element (DOE) that is formed as part of base wafer 118. DOE 113 can be patterned from a stack of phase shifting layers separated by etch stop layers to the desired lens shape. The phase shifting layers can be amorphous silicon (α-Si) and the etch stop layers can be silicon dioxide (SiO_2). Alternatively, the phase shifting layers can be silicon nitride (Si_3N_4) instead of amorphous silicon.

[0014] To form the stack, an amorphous silicon layer is first formed on substrate 118. The amorphous silicon layer can be deposited by low pressure chemical vapor deposition (LPCVD) or by plasma enhanced chemical vapor deposition (PECVD). A silicon dioxide (SiO_2) layer is next formed on the amorphous silicon layer. The silicon dioxide layer can be thermally grown on the amorphous silicon layer in steam at 550°C or deposited by PECVD. The process of forming the amorphous silicon and silicon dioxide layers is repeated for the desired number of phase shift layers. Once the stack is formed, the amorphous silicon layer is masked and then etched down to the next silicon dioxide layer, which acts as the etch stop. The process of masking and etching is repeated for the remaining phase shifting layers to form DOE 113.

[0015] Bonding pad 120 forms a perimeter around package 100 corresponding to gasket 106. Contact pad 122 provides an electrical connection to optoelectronic device 120. In one embodiment, bonding pad 120 and contact pad 122 are Au deposited by sputtering, evaporation, or plating, and patterned by masking and etching or liftoff. A barrier metal layer (not shown) can be formed between base wafer 118 and pads 120 and 122 to act as a diffusion barrier and to improve adhesion between the pad material and the base wafer material.

[0016] Optoelectronic device 102 is located on base wafer 118. Optoelectronic device 102 is electrically connected to contact pad 122 by a wire bond, a solder bump bond, a flip chip technique, or other attachment techniques. Depending on the embodiment, optoelectronic device 102 can be an edge-emitting laser (e.g., a Fabry-Perot or a distributed feedback (DFB) laser) or a vertical cavity surface-emitting laser (VCSEL). If it is an edge-emitting laser, optoelectronic device 102 is typically a separate die that is aligned and bonded to base wafer 118. If it is a VCSEL, optoelectronic device 102 can be grown directly on base wafer 118.

[0017] Base wafer 118 can include additional elements, such as a power monitor (e.g., a photodiode), leads (e.g., buried traces) for electrical connectivity, and other active and passive circuitry.

[0018] Referring to Fig. 2, cap wafer 104 is aligned and bonded to base wafer 118. Depending on the embodiment, the seal between cap wafer 104 and base wafer 118 may or may not be hermetic.

[0019] In one embodiment, an Au/Au thermocompression bond is formed between gasket 106 and bonding pad 120. This thermocompression bond is formed by simultaneously applying both temperature and pressure for a predetermined time (e.g., between 30 to 120 megapascals from 320 to 400°C for 2 minutes to 1 hour). In this embodiment, the barrier metal layer for Au on gasket 106 and bonding pad 120 can be (1) a titanium tungsten (TiW)/titanium tungsten nitrogen oxide (TiWNO)/TiW tri-layer, (2) titanium/platinum bi-layer, (3) chromium/platinum bi-layer, (4) tungsten silicon nitride, (5) titanium silicon nitride, (6) silicon dioxide/titanium bi-layer, (7) silicon dioxide/chromium bi-layer, or (8) silicon dioxide/titanium tungsten bi-layer. The barrier metal layer can be deposited by sputtering or evaporation and patterned by masking and etching or liftoff. The barrier metal layer should provide a good diffusion barrier and act as a good adhesion layer between Au and Si, which in-turn yields a clean Au/Au bond.

[0020] In another embodiment, an Au/Si reaction bond is formed between gasket 106 and bonding pad 120. This reaction bond is formed by simultaneously applying both temperature and pressure for a predetermined time (e.g., between 60 to 120 megapascals from 300 to 365°C for 5 to 30 minutes). In this embodiment, the barrier metal layer is replaced with an adhesion layer such as Ti so Au and Si on cap wafer 104 and base wafer 118 can interdiffuse and react to form a bond consisting of a gold-silicon mixture.

[0021] In yet another embodiment, an Au/Sn solder bond is formed between gasket 106 and bonding pad 120.

[0022] The choice of the bonding material and the type of the bond between cap wafer 104 and base wafer 118 depends on a number of factors, including adhesion requirements, hermeticity requirements, and the ability of optoelectronic device 102 and other integrated electronics to tolerate bonding conditions. For example, if optoelectronic device 102 is an edge-emitter laser attached to base wafer 118 by a solder bond, then a thermocompression

bond at a high temperature can lead to solder reflow that causes the laser to misalign. Consequently, a solder bond for the cap wafer 104 may be more appropriate.

[0023] Referring to Fig. 3, a via contact (or plug) 142 and a via contact pad 144 are formed to provide an electrical connection to optoelectronic device 102. In one embodiment, the topside of cap wafer 104 is grinded to expose via 110 (Figs. 1 and 2). Via 110 is then widened by an isotropic etch. Metal is then formed in and around via 110 to form via contact 142 and contact pad 144, which are electrically connected to contact pad 122. In one embodiment, a metal barrier/adhesion layer is deposited by sputtering or evaporation on cap wafer 104 and sidewalls of via 110 and then patterned by masking and etching or liftoff. Via contact 142 and contact pad 142 are next formed by electroplating Au over the metal barrier/adhesion layer. Alternatively, via contact 142 is Au deposited by sputtering or, evaporation. Contact pad 144 can then be patterned by masking and etching or liftoff to form the desired shape.

[0024] In one embodiment, an edge-emitting laser 102 emits a light 146 that is reflected downward by mirror 118. Light 146 then exits package 100 through base wafer 118. If base wafer 118 is silicon, then package 100 is applicable to a single-mode transmitter operating in the 1300 nm regime in which silicon base wafer 118 is transparent.

[0025] Figs. 4, 5, and 6 are cross-sections of a wafer-level package 200 (Fig. 6) for an optoelectronic device 202 in one embodiment of the invention.

[0026] Referring to Fig. 4, package 200 includes a cap wafer 204 having gaskets 106 and 108, vias 110, a cavity 212, and an integrated lens 213.

[0027] Cap wafer 204 can be Si, GaAs, InP, or other similar materials. Gaskets 106 and 108 and via 110 are formed as described above. Cavity 212 is formed by masking and etching cap wafer 204.

[0028] In one embodiment, integrated lens 213 is a diffractive optical element (DOE) that is formed as part of cap wafer 204 as described above with integrated lens 113.

[0029] Referring to Fig. 4, package 100 further includes a base wafer 218 having bonding pad 120 and contact pads 122. Bonding pad 120 and contact pads 122 are formed as described above.

[0030] Optoelectronic device 202 is located on base wafer 218. Depending on the embodiment, optoelectronic device 202 can be an edge-emitting laser (e.g., Fabry-Perot or DFB) or a VCSEL. If it is an edge-emitting laser, optoelectronic device 202 is aligned and bonded to base wafer 218. If it is a VCSEL, optoelectronic device 202 can be grown directly on base wafer 218.

[0031] Base wafer 218 can include additional elements, such as a power monitor (e.g., a photodiode), leads (e.g., buried traces) for electrical connectivity, and other active and passive circuitry.

[0032] Referring to Fig. 5, cap wafer 204 is aligned and bonded to base wafer 218. Gasket 106 can be bonded to bonding pad 120 by a thermocompression, a reaction bond, or a solder bond as described above.

[0033] Referring to Fig. 6, via contacts 142 and via contact pads 144 are formed to provide electrical connections to optoelectronic device 202. Via contacts 142 and contact pads 144 are formed as described above.

[0034] As shown in Fig. 6, a VCSEL 202 emits a light 246 through DOE 213 in cap wafer 204. If cap wafer 204 is silicon, then package 200 is applicable to a single-mode transmitter operating in the 1300 nm regime in which silicon is transparent.

[0035] There are a number of advantages to the invention described above over currently existing packaging techniques. These include, but are not limited to, reduced labor costs with a significant reduction in product cost, potentially faster cycle times, and the ability to easily scale to high volume manufacturing.

[0036] Various other adaptations and combinations of features of the embodiments disclosed are within the scope of the invention. Numerous embodiments are encompassed by the following claims.